

This diagram shows a cross-sectional view of a multi-layered semiconductor device. It features a base layer 22 at the bottom, which is divided into two horizontal sections. Above the base are four patterned layers: 24, 25, 26, and 27. Layer 24 is the bottommost patterned layer, followed by 25, 26, and 27. A top layer 28 is positioned above layer 27. Conductive vias, labeled 29 and 29', are used to connect the different layers. Specifically, vias 29 connect the top surface of layer 24 to the top surface of layer 25, and vias 29' connect the top surface of layer 26 to the top surface of layer 27. A lead 26 is shown on the right side of the device, connected to the top surface of layer 24.

Fig. 3

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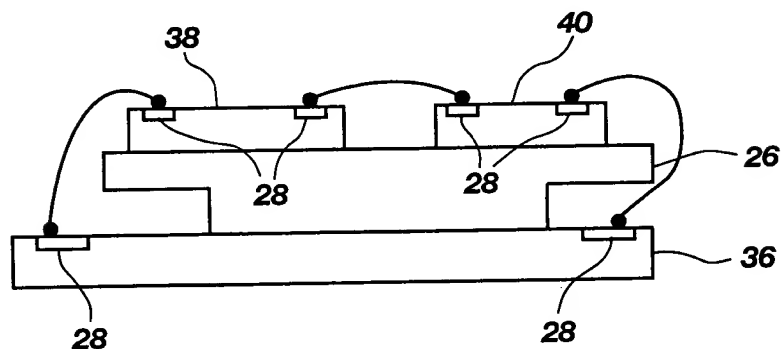


Fig. 4

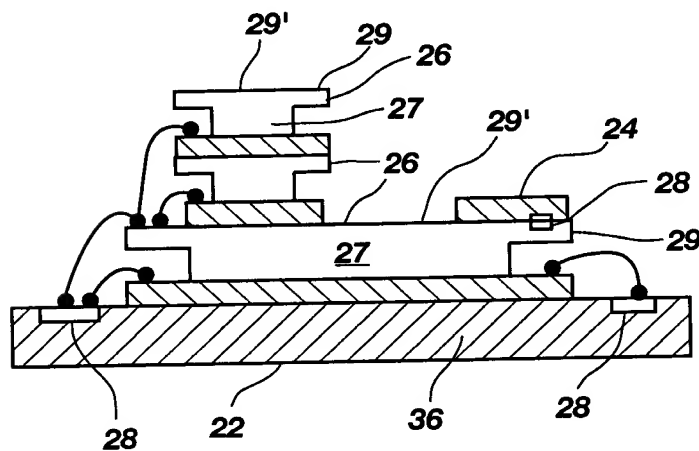


Fig. 5

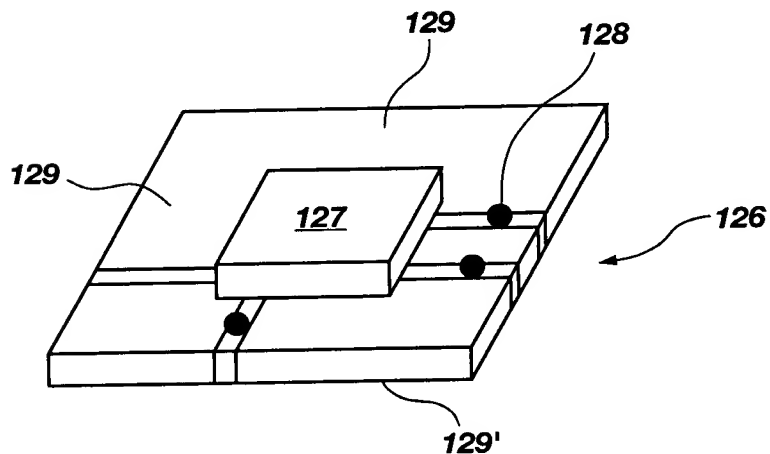


Fig. 6

FIG. 4

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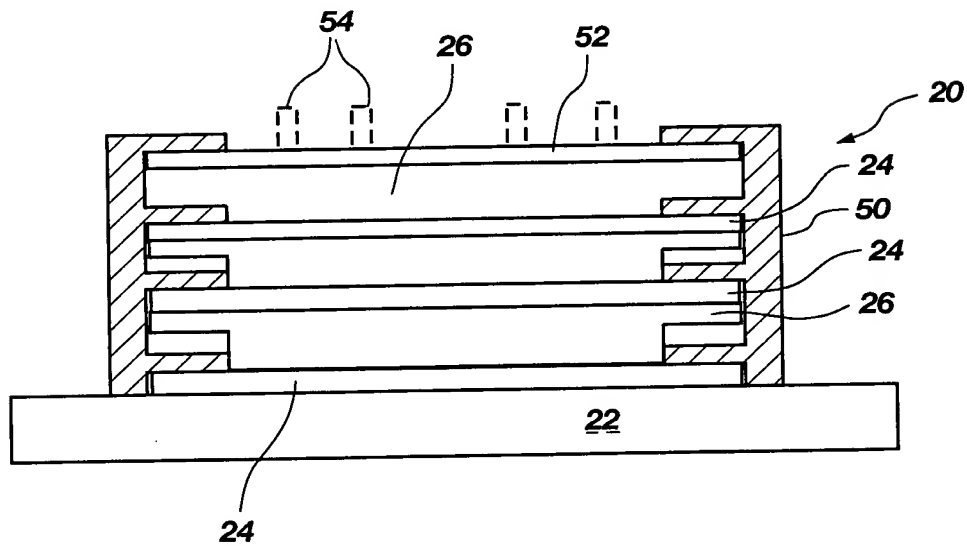
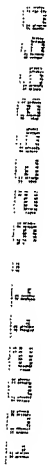
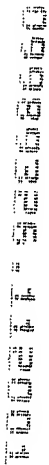


Fig. 7

FIG. 7 - SEE 0003/5



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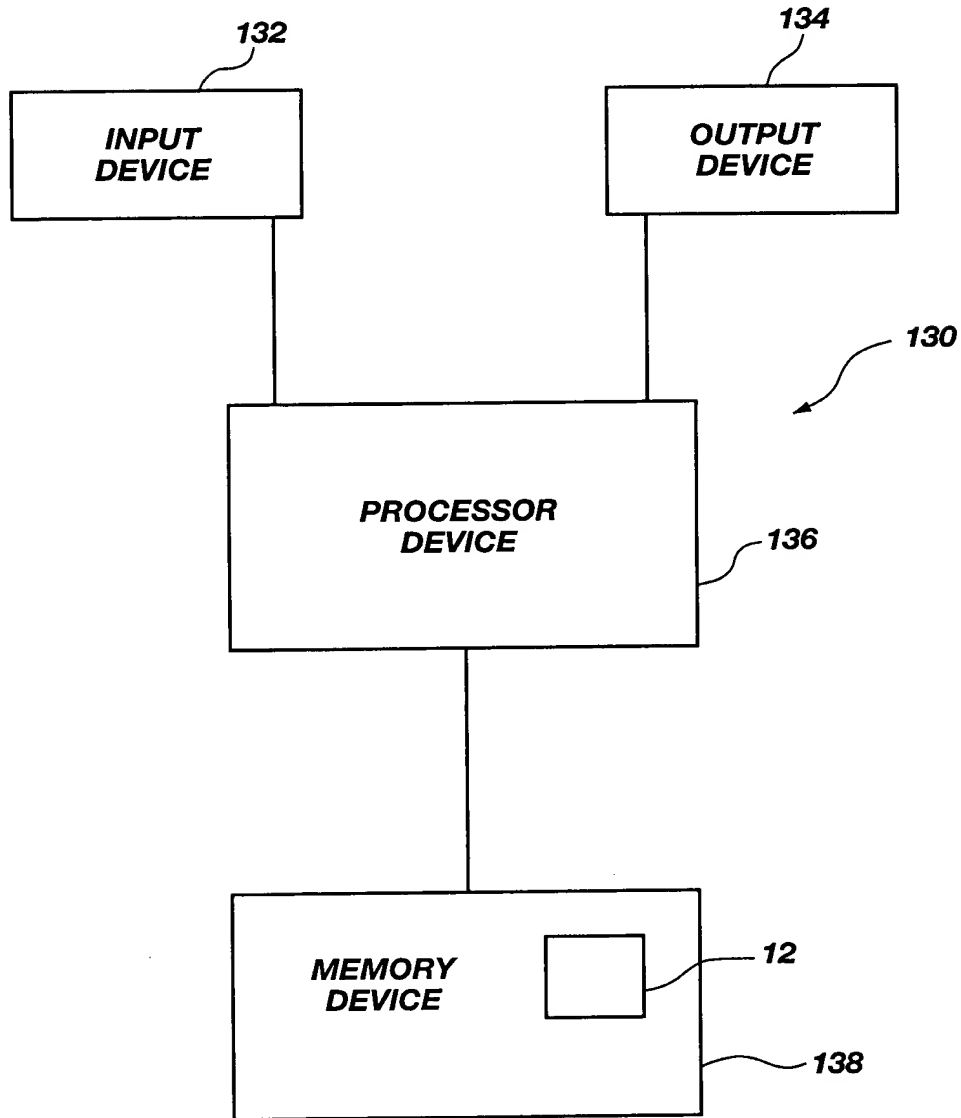


Fig. 10